GOVERNMENT COLLEGE OF ENGINEERING, AURANGABAD

(An Autonomous Institute of Government of Maharashtra)

Department of Electronics& Telecommunication Engineering

End Semester Examination (Semester I)

Class: ME (1st Yr.) in Electronics Engineering **Date:**

Subject: ET 545 VLSI Design **Time:** 17 DEC 2016 **Max. Marks:** 60

a) Question 1 and 4 are compulsory
b) For Question 2, 3, 5, 6, answer two out of three
c) Assume suitable constants where not provided
d) Question 1 and 4 are of 10 Marks each (M 10)
e) Each answer in 2,3,5,6 is 5 marks each (M 5)

Q1. List and explain various layout constraints in CMOS Layout. M 10

Q2. Write short notes on two of the following three

g) Noise Margins in CMOS Inverter M 5
h) Low Power CMOS Design M 5
i) Shot Channel Effects M 5

Q3. Answer any two of the following three

g) What is channel length modulation? M 5
h) If you reduce the size of NMOS device to half, what does this do to device performance? M 5
i) Vgs=0.6V, Vt=0.42V, Ids=500uA, what is the drain current at 0.7V? M 5

Q4. How do you overcome the effects of Technology Scaling? M 10

Q5. Write short notes on two of the following three

g) Cost of Digital Logic M 5
h) Boolean Algebra and Duality M 5
i) High Speed Interconnects M 5

Q6. Answer any two of the following three

g) Draw a simple sense amplifier based D Latch. M 5
h) What is the role of delay in Master Slave D register? M 5
i) Design a circuit for dual edge Pulse Generator. M 5

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